Operating Margins of a 10 V Programmable Josephson Voltage Standard Circuit Using $\mathrm{NbN/TiN}_x\mathrm{/NbN/TiN}_x\mathrm{/NbN}$ Double-Junction Stacks

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***Abstract*—The operating margins of a 10 V programmable Josephson voltage standard circuit using $\mathrm{NbN/TiN}_x\mathrm{/NbN/TiN}_x\mathrm{/NbN}$ double-junction stacks was investigated as a function of microwave frequency and operating temperature. The circuit contained 32 arrays of 5 120 $\mathrm{NbN/TiN}_x\mathrm{/NbN/TiN}_x\mathrm{/NbN}$ double-junction stacks. In other words, the circuit contained 327 680 $\mathrm{NbN/TiN}_x\mathrm{/NbN}$ junctions. It was found that the operating margins (the heights of the constant-voltage step) of the arrays varied largely with microwave frequency and operating temperature. The microwave-frequency dependence was due to the resonance of the microwaves in the circuit. The temperature dependence of the circuit was due to the temperature dependence of the I_cR_n product of the junctions, where I_c was the critical current and R_n was the normal resistance. Fortunately, however, the operating margin was maximized by changing the temperature of the chip, mounted on the cold head of a cryocooler.**

***Index Terms*—Cryocooler, margin, NbN, PJVS, TiN_x.**

I. Introduction

A programmable Josephson voltage standard (PJVS) [1]–[8] using a superconductor / normal-metal / superconductor (SNS) Josephson junction is possibly a next generation Josephson voltage standard, due to its advantages over a conventional voltage standard. The PJVS has two main advantages; first, the programmable output voltage provided by a digital to analog converter (DAC) function, and second, the high tolerance to noise due to the large current margins of the Josephson array.

Benz *et al.*. demonstrated a programmable 1V Josephson voltage standard using Nb/PdAu/Nb junctions with an I_cR_n product of about 30 μV, corresponding to a characteristic frequency of 15 GHz [3]. Schulze *et al.*. reported the fabrication of junction arrays for a 10V PJVS with a 200 μA step width, which included 69 120 $\mathrm{Nb/AlO}_x\mathrm{/Al/AlO}_x\mathrm{/Nb}$ junctions [5]. Chong *et al.*. demonstrated a 3.87 V maximum output voltage with a practical operating current margin greater than 1 mA using triple-stacked junctions with MoSi2 barriers [8].

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In this study a DAC employing an $\mathrm{NbN/TiN}_x\mathrm{/NbN/TiN}_x\mathrm{/NbN}$ double-junction stacks was developed as a PJVS, cooled using a cryocooler to about 10 K. While Nb-based circuits were also operated with a cryocooler at 4 K [9], [10], the higher operating temperature of the NbN-based PJVS was found to reduce the electric power consumption and total volume of the system, also resulting in cost reduction [11]. If a desktop PJVS could be produced as an inexpensive commercial product, it would not only be employed at research centers as a primary standard but also at other research laboratories and factories.

The current development program of the PJVS was started in collaboration with the National Institute of Standards and Technology (NIST). The NbN-based PJVS circuits were designed based on Nb-based PJVS circuits. They were continuously modified and optimized for NbN junction technology. An 8 bit 1 V PJVS was demonstrated using $\mathrm{NbN/TiN}_x\mathrm{/NbN}$ junctions cooled with a cryocooler to 10 K [12]. A 10 V PJVS based on NbN junctions was also tried to be demonstrated. The double-junction stack [13]–[15] was necessary to integrate the large number of junctions for a 10 V output voltage with a practical chip size of 15 mm $\times$ 15 mm. Although there were many problems related to low fabrication yield and poor microwave characteristics, 10 V output voltage with approximately 1 mA margins was demonstrated [18].

In this paper, we describe a fully operational 10V programmable Josephson voltage standard, operating at about 10 K. We also present details describing the interdependencies of the experimentally measured operating margins on temperature and frequency. These parameters can be used as a guide to find maximum operating margins.

II. Circuit Design

Fig. 1 is the equivalent circuit of the 11 bit DAC design for the 10 V PJVS. Fig. 2 is a photograph of the fabricated chip. In the chip, 163 840 $\mathrm{NbN/TiN}_x\mathrm{/NbN/TiN}_x\mathrm{/NbN}$ double junction stacks were divided into 32 parallel arrays. Each array contained 5 120 double-junction stacks. For DAC operation, the total series-connected array containing 163 840 stacks was divided into 22 cells with 23 bias taps. The number of stacks in each of the 22 cells was: 160, 160, 320, 640, 1 280, 2 560, 5 120 and 15 cells with 10 240 stacks. The 23 bias taps were connected to the array through 16 GHz quarter-wavelength transformers for microwave blocking. The size of the junctions was 3.4 μm $\times$

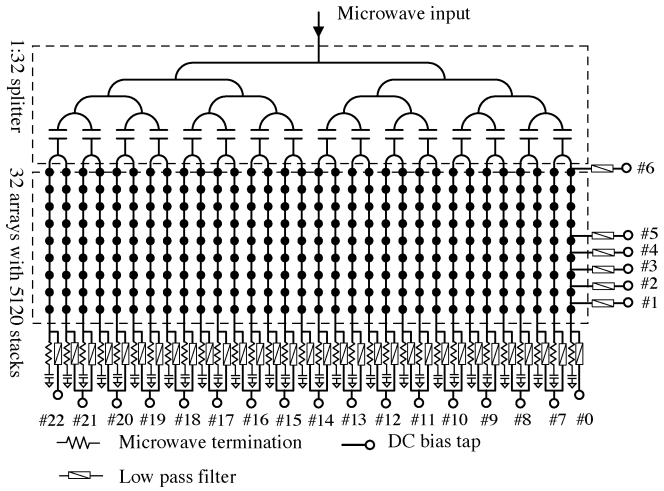

Fig. 1. Equivalent circuit of a 10 V PJVS circuit.

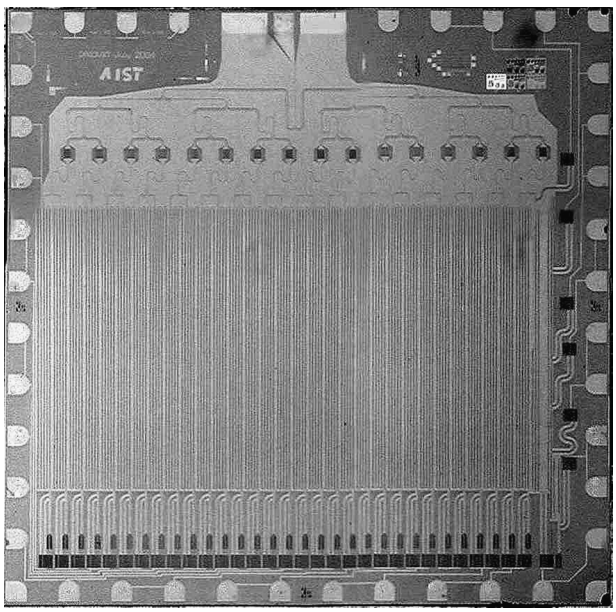

Fig. 2. Photograph of a 10 V PJVS chip containing 327 680 Josephson junctions. The chip size is 15 mm × 15 mm.

3.4 μm. The critical current density was about 7×10^8 A/m^2. The DAC chip was designed to use one tap to launch the microwave. The microwave was equally split between the 32 arrays through a coplanar network circuit and dc blocking capacitors. A 16 GHz quarter-wavelength coplanar waveguide (CPW) with a specific impedance of 36 Ω was connected to two 50 Ω CPWs, which functioned as 2-way splitters. Five consecutive stages of the 2-way splitters were connected in series in order to divide the microwave into 32 arrays. A formula to estimate the characteristic impedance for the CPW made of metal may not be available for that made of NbN due to its large kinetic inductance [16]. Therefore, the center line width and the space between the center and outer conductors for both the 36 and 50 Ω CPWs were optimized using electromagnetic field simulations, taking into account the kinetic inductance of the NbN film [17]. This optimization of the characteristic impedance significantly reduced the microwave power required to obtain a 1-mA wide step from 1 W to 400 mW.

TABLE I
A SUMMARY OF LAYERS

Layer	Material	Thickness (nm)
Etch stop	Al	2
Base electrode	NbN	300
1st barrier	TiN_x	24
Middle electrode	NbN	40
2nd barrier	TiN_x	24
Counter electrode	NbN	200
Resistor	Pd	40
Isolation	SiO_2	400
1st Wiring	NbN	500
2nd Wiring	NbN	500
Passivation	SiO_2	200

III. FABRICATION

Here, we describe a fabrication process for the PJVS chip, although it was reported in previous paper [18]. The typical thickness of each layer of the device is summarized in Table I. The fabrication process is described in the following steps: (1) An Al film as an etch stop and an $NbN/TiN_x/NbN/TiN_x/NbN$ multilayer were consecutively deposited using reactive rf sputtering on a Si wafer of a 3 inch diameter; (2) The counter electrode NbN film, two TiN_x barriers, and a middle electrode NbN were patterned using reactive ion etching (RIE), the thickness of the TiN_x barrier was 24 nm, predefined to provide an I_cR_n of 33 μV at 10 K; After the patterning procedure, the photoresist, polymer, and particle on the wafer were removed both chemically and mechanically using N-Methyl- 2-Pyrrolidone (NMP) jet; (3) the base electrode was patterned using RIE, the Al layer for etch stop was removed using NMP jet; (4) a Pd film was sputter-deposited and patterned for fabricating the termination resistors, the patterning was performed using the lift-off method; (5) an SiO_2 film as the electrical isolation was deposited using rf sputtering; (6) via holes were formed from reactively ion etching the SiO_2 layer and a portion of the counter-electrodes; (7) an NbN film was deposited, however, because of the previously patterned structures, this NbN film was not flat; (8) in order to avoid a significant reduction in the wiring critical currents, the surface of the NbN wiring was planarized through Chemical- Mechanical polishing (CMP) [19], [20]; (9) an additional NbN film was deposited; (10) the film was patterned using RIE; (11) finally, an SiO_2 film as a passivation layer was deposited and contact holes to the dc bias pad were formed using RIE.

The CMP was introduced to avoid a significant reduction in the wiring critical current $I_{\max}$. In addition a wide base electrode (16 μm) was employed to avoid a reduction in $I_{\max}$ due to heat generated from the junction array [21].

For several years, we have attempted to improve the fabrication yield of the PJVS circuit. A significant factor in the low fabrication yield was the poor insulation performance of the SiO_2 films which caused short circuits between the metal layers. The major cause of the pin holes in the SiO_2 films was found to be contamination of the surface of the base electrode due to

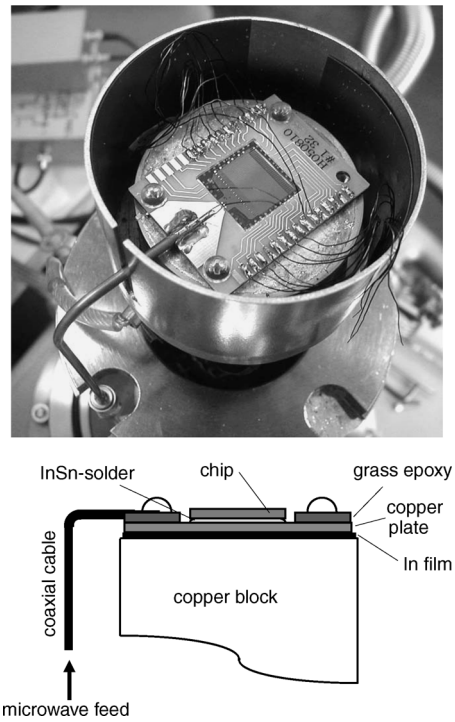

Fig. 3. Photograph and illustration of the cross section of a chip mounted on a copper plate.

high humidity in our clean room. We observed that the fabrication yield depended on the seasons, that is, the fabrication yield dropped during the rainy season in Japan. To overcome the problem, a new air-conditioning system was installed into the clean room so we can now reliably maintain a relative humidity of about 50%. Furthermore, we also tried to use an interdigitated capacitor instead of a parallel plate capacitor, susceptible to pin holes in the SiO_2 film.

IV. Packaging

In our previous report, the chip was mounted to the chip carrier using flip chip bonding to make good thermal contact between the chip and the cold head of the cryocooler [12]. It was also reported that this method improved the operating margins [22]. However, there were some difficulties in the formation of the uniform solder bumps, and in the precise alignment of the chip to the chip carrier. Furthermore, it was found that when pressure was applied to the chip carrier to make good thermal contact, the chip could easily break. Thus, the flip chip bonding was discarded and another method that did not require high mechanical force was introduced. As shown in Fig. 3, the back of the chip was bonded to a 30 mm $\times$ 40 mm copper plate with InSn solder to make good thermal contact. It was necessary to have a sputter-deposited gold film at the back of the Si chip because InSn solder debonded from Si when there was no metal buffer. The printed circuit board (PCB) and the chip were connected using Al wire bonding. The chip carrier consisted of the PCB, the chip and the copper plate, and was mounted on a copper block with screws. The chip was cooled to about 10 K using a two-stage Gifford-McMahon cooler with a refrigeration capacity of 1.4 W at 10 K.

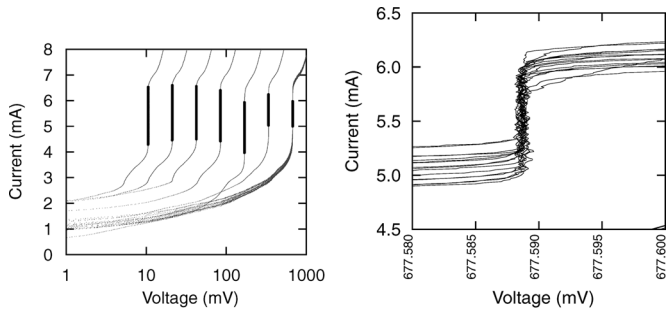

Fig. 4. (a) Current-voltage $(I-V)$ characteristics of 22 array cells from the 11 bit 10 V PJVS circuit, using double-junction stack arrays. All $I-V$ s were measured at 200 mW, 16 GHz. The chip was cooled using a cryocooler to 9.7 K. The multiple overlapping $I-V$ s with the largest voltage step correspond to the 15 array cells, each having 20 480 junctions. (b) Overlaid current voltage curves for the largest 15 cells, showing overlapping $n=1$ steps that are flat within measurement noise. The largest cell is combined from 2 arrays, each containing 5 120 stacks (10 240 junctions).

A 0.5-m long coaxial cable was used inside the cryocooler to connect the chip carrier and the SMA terminal located outside of the cryocooler. The choice of the material for the coaxial cable inside the cryocooler to launch the microwave was important because a good conductor of electricity is also a good conductor of heat. We tried three types of coaxial cables whose outer conductors were made of different materials: Cu; Ag-coated CuNi; and Cu-coated stainless steel. The temperature at the cold head increased more than 3 K when the Cu coaxial cable was used. The Ag-coated CuNi cable did not raise the temperature of the cold head. However, the attenuation of the 16 GHz microwave was more than 10 dB/m. The attenuation of the microwave in the Cu-coated stainless steel cable was about 5 dB/m. The increase in the temperature of the cold head was negligible. Therefore, the Cu-coated stainless steel cable was chosen to be employed in the measurement system.

V. Experimental Measurements

A. Array Size Dependence

Fig. 4(a) is the current-voltage $(I-V)$ characteristics of the 22 array cells of an 11-bit PJVS circuit fabricated using double-junction stack arrays. All $I-V$ s were measured at 200 mW, 16 GHz, where the microwave power was measured at the output terminal of the microwave source. During measurement the chip was cooled with a refrigerator to 9.7 K. The multiple overlapping $I-V$ s in the figure are of the largest voltage step, correspond to 15 array cells having 20 480 junctions each. Fig. 4(b)is the overlaid $I-V$ curves for the largest 15 cells, showing overlapping $n=1$ steps that are flat, within measurement noise. The largest cell consists of two arrays, containing 5 120 stacks (10 240 junctions) each. A summary of the current margins of each cell is presented in Table II. The maximum and minimum values of the margins are 2.13 and 0.73 mA, respectively.

Fig. 5 is a plot of the height of $n=1$ steps as a function of the number of Josephson junctions included in the junction arrays. The microwave frequency was 16 GHz, and the operating temperature was chosen so that the I_cR_n product became

TABLE II
A SUMMARY OF THE MARGINS

Sample ID : H051012#2				
Channel	Number of junctions	The $n = 1$ step (mA) min	max	width
0	1280	4.47	6.51	2.04
1	320	4.30	6.43	2.13
2	320	4.33	6.43	2.10
3	640	4.46	6.52	2.06
4	2560	4.43	6.30	1.87
5	5120	3.98	5.87	1.89
6	10240	5.04	6.16	1.12
7	20480	5.23	6.20	0.97
8	20480	5.06	6.12	1.06
9	20480	4.97	6.11	1.14
10	20480	5.11	6.12	1.01
11	20480	5.17	6.11	0.94
12	20480	5.33	6.09	0.76
13	20480	5.31	6.05	0.74
14	20480	5.10	5.99	0.89
15	20480	5.02	6.05	1.03
16	20480	5.01	5.96	0.95
17	20480	5.18	5.91	0.73
18	20480	5.20	5.96	0.76
19	20480	5.12	5.99	0.87
20	20480	4.96	6.04	1.08
21	20480	4.98	6.09	1.11

Current margins (mA)	
min	0.73
max	2.13
overlap	0.54

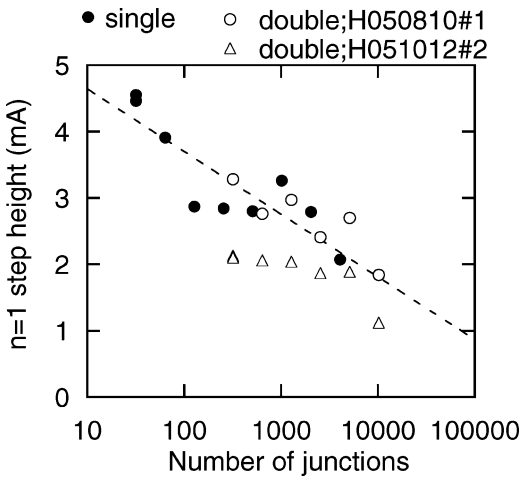

Fig. 5. Relation between the $n = 1$ step height and the number of junctions per array for single- and double-junction stack.

about 33 μV. The critical currents were approximately 5 mA. In this figure, the margins outlined in Fig. 4 are plotted using open triangles. These margin data are found to be only slightly lower than those (plotted as open circles) reported in [18]. As the number of junctions was increased, the $n = 1$ step height was found to decrease. The decrease of the step height in dependence of the junction number can be due to both parameter spread and microwave damping [23]. The larger number of parallel arrays with smaller number of junctions can be one of solutions to improve operating margins [24]. For comparison, in Fig. 5, the margins of singlejunction arrays of a 1 V PJVS circuit are plotted (closed circles). Although they can not be exactly

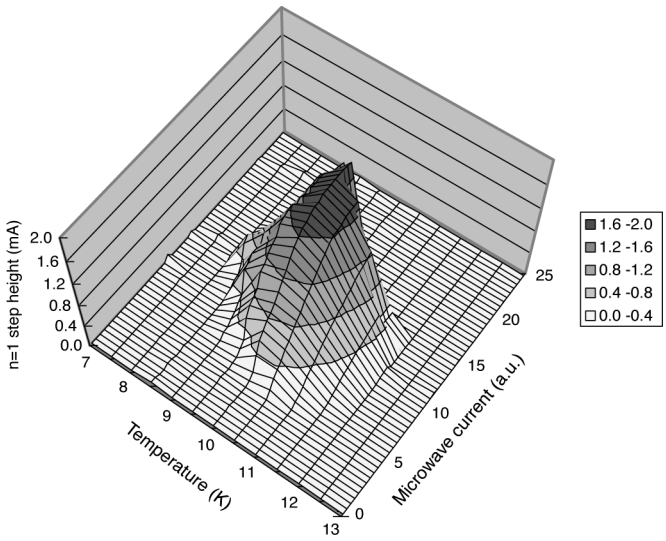

Fig. 6. Measured operating current margins as a function of the temperature and microwave current for one of the largest 15 cells.

compared due to differences in design, there are no significant differences between the single- and double- junction arrays.

B. Uniformity and Margin

The margins of the double-junction stack depended on the uniformity of the critical current I_c between the upper and lower junctions in the stack. The variation in I_c shown in Fig. 4 was less than 10%. Although the mechanism for the variation is not clearly identified, the upper junction tended to exhibit a larger I_c than the lower junction [13]. It is suggested that an increase in temperature during the sputter deposition process could have caused the observed variation. To obtain identical critical current we warm up the sputter machine by depositing to a dummy wafer before sputter-deposition of the junction stack. The variation in uniformity between fabrications (run-to-run variation) also remained as a problem.

C. Temperature Dependence

Fig. 6 is the measured $n = 1$ step height as a function of the temperature and microwave current for one of the largest 15 cells; the dc bias current was supplied between the dc bias taps #7 and #8; these numbers are marked in Fig. 1. The frequency of the applied microwaves was fixed at 16 GHz. The output voltage was measured between the dc bias taps #0 and #22. When the applied microwave current was increased to more than about 15 (a.u.), the step was suddenly suppressed. Although the cause is still not known, this result suggests that a small critical current exists along the wiring and may be the cause.

Kautz discussed the operating margins of Josephson junction arrays from a theoretical standpoint [25]. He concluded that junctions have an optimum operating frequency $\Omega(= f/I_cR_nKj) \approx 1$, where $K_{\rm j} = 2e/h$ while $483\ 597.9\ {\rm GHz/V} = K_{\rm j-90}$. Borovitskii *et al.* reported that the greatest tolerance of step position to critical current variation in arrays is obtained for $\Omega \approx 1$ [26]. Experimentally obtained results presented in Fig. 6 agree with these theoretical

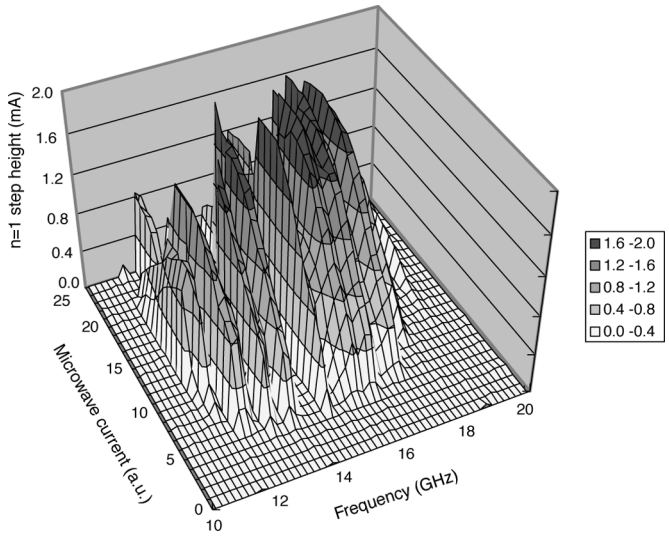

Fig. 7. Measured operating current margins as a function of the microwave current and frequency for one of the largest 15 cells.

predictions. The normal resistance R_n was found to be independent of temperature; the frequency f was fixed at 16 GHz. Therefore, the reduced frequency Ω was only a function of the critical current I_c. The critical current I_c is dependent on the temperature, and thus suggests that the optimum Ω of $\approx$1 can be obtained by changing the temperature. The I_cR_n product is usually controlled by changing the barrier thickness of the Josephson junction. However, there is a run-to-run variation in this thickness, which results in the variation in I_cR_n. When the operating temperature is fixed, we have to choose a wafer that exhibit an appropriate I_cR_n. After introducing the cryocooler, the I_cR_n product could be changed by adjusting the operating temperature to maximize the current margins. This is a significant advantage of the use of the cryocooler, which is also effective with the Nb-based circuits operated at 4 K [9], [10].

D. Frequency Dependence

Fig. 7 is the measured $n = 1$ step height at 9.7 K as a function of the microwave current and frequency for one of the largest 15 cells; the dc bias current was supplied between the dc bias taps #7 and #8.

It is clear from this data that the optimum microwave frequency is approximately 16 GHz. Although the magnitude of the step height was dependent on the temperature, this optimum frequency was identical at different temperatures (9.7$\pm$1.0 K). This indicates that the optimum frequency does not depend on the I_cR_n product. The optimum frequency may be defined from the microwave circuits used for the on-chip splitter and the low pass filters [27].

The frequency dependence in Fig. 7 also indicates that there is a problem to be solved. Many fine structures appeared when the frequency was swept. These structures may be due to undesirable resonances in the microwave circuit, and may degrade the operating margin. These margins on frequency are very important because a continuous voltage adjustment is required for certain applications. As the LSB has 320 junctions, the minimum voltage resolution is about 10 mV for a fixed frequency. The frequency must be sufficiently changed to get any voltage. In this study we used the interdigitated capacitor to avoid a short circuit problem. However, we found that the low-pass filter with the interdigitated capacitor yielded resonant peaks in the frequency dependence of the operating margin due to a stray inductance in the capacitor [28]. A resonance free low pass filter [29] must be used to avoid such a problem.

VI. Conclusion

In summary, a 10 V PJVS circuit cooled with a cryocooler to 10 K was successfully demonstrated, with a practical operating margin. Although there was a run-to-run variation in the uniformity of the double-junction stacks, the nearly equal current margins for the $n = 1$ steps compared to the single junction were obtained. It was found that the operating margin was maximized when the reduced frequency $\Omega \approx 1$, namely $I_cR_n \approx 33\ \mu$V. That is, we can maximize the operating margins by changing the operating temperature of the cryocooler instead of fabricating chips that make use of a different barrier thickness. This advantage of operation with a cryocooler is quite attractive for its practical application.

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